

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	((("6263426") or ("6292815") or ("6247116") or ("6266769")).PN.	US-PGPUB; USPAT	OR	OFF	2006/06/16 09:48
L2	1	("5450607").PN.	US-PGPUB; USPAT	OR	OFF	2006/06/16 10:01
L3	526	((712/221) or (708/204)).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/06/16 10:07
L4	447	(712/210).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/06/16 10:07
L5	441	(decod\$3 (int or integer) (fp or floating near3 point) (pack\$3 or unpack\$3) register architectural conver\$4 format)	USPAT	AND	ON	2006/06/16 10:09
L6	5	(decod\$3 (int or integer) (fp or floating near3 point) (pack\$3 or unpack\$3) register architectural conver\$4 format).clm.	USPAT	AND	ON	2006/06/16 10:09



Welcome United States Patent and Trademark Office

☐ Search Session History[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Fri, 16 Jun 2006, 9:42:22 AM EST

Edit an existing query or
compose a new query in the
Search Query Display.

Search Query Display

Select a search number (#)
to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

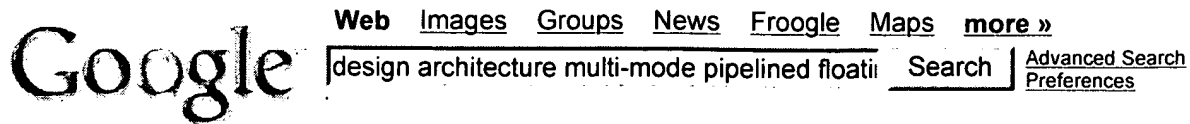
Recent Search Queries

- [#1](#) (darley<in>au)
- [#2](#) ((darley<in>au) <and> (sparc<in>ti))
- [#3](#) ((darley<in>au) <and> (sparc<in>ti))
- [#4](#) ((gilliam<in>au) <and> (pipelined<in>ti))
- [#5](#) (gilliam<in>au)
- [#6](#) (gilliam<in>au)
- [#7](#) (design and archtecture multi-mode<in>ti)
- [#8](#) (gilliam x.<in>au)
- [#9](#) (gilliam r.<in>au)
- [#10](#) (gilliam j. e.<in>au)
- [#11](#) (gilliam f. t.<in>au)
- [#12](#) (design architecture multi-mode pipelined<in>metadata)

Indexed by
 Inspec

[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2006 IEEE –

[Sign in](#)

Web Results 1 - 10 of about 377 for **design architecture multi-mode pipelined floating-point adder**. (0.60 s)

Did you mean: design architecture **multimode** pipelined floating-point adder

[PDF] **Design and architecture for a multi-mode pipelined, floating-point ...**

File Format: PDF/Adobe Acrobat

Page 1. Page 2. Page 3. Page 4.

ieeexplore.ieee.org/iel2/ 566/4267/00165725.pdf?arnumber=165725 - [Similar pages](#)

Welcome to IEEE Xplore 2.0: **Design and architecture for a multi ...**

Design and architecture for a multi-mode pipelined, floating-point adder ... IEEE Standard VLSI **floating-point adder** block **floating-point** double-precision ...

ieeexplore.ieee.org/xpls/absprintf.jsp?arnumber=165725 - [Similar pages](#)

[[More results from ieeexplore.ieee.org](#)]

Unified floating point and integer datapath for a RISC processor ...

"**Design and Architecture for a multi-mode pipelined, floating-point adder**", May 1991;

IEEE. Enriquez et al. "**Design of a multi-mode pipelined multiplier for ...**

www.freepatentsonline.com/5450607.html - 39k - [Cached](#) - [Similar pages](#)

[PDF] **The VEGA Moderately Parallel MIMD, Moderately Parallel SIMD ...**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

Processing element **design**. The **architecture** of the individual PE is of course an im- ...
ister file, and a **pipelined** bit-parallel **floating point** ALU. ...

ipdps.cc.gatech.edu/1998/papers/259.pdf - [Similar pages](#)

GSPX

Design of a Multi-Mode Channel - Select and Resampling-Processor (ASIP)- SoC - D ...

Time Efficient 32 Bit **Floating Point Adder** for Intelligent System ...

www.gspx.com/index.php?op=ad_click&bid=2 - 108k - [Cached](#) - [Similar pages](#)

[PDF] **Curriculum Vitae – Michael J. Flynn**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

Computer **Architecture: Pipelined** and Parallel Processor **Design**. Jones and Bartlett, Boston, ... **Design** and Implementation of the SNAP **Floating-Point Adder**. ...

arith.stanford.edu/~flynn/flynnvcv.pdf - [Similar pages](#)

[PDF] **Applications of Small-Scale Reconfigurability to Graphics Processors**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

the entire graphics **pipeline** for the SSR **architecture**. ... A dual-mode **floating point** unit is a small-scale reconfigurable unit capable of ...

www.cs.virginia.edu/papers/ssr_gpu_arc2006.pdf - [Similar pages](#)

[PDF] **Applications of Small Scale Reconfigurability to Graphics Processors**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

precision **floating point** units, morphable multipliers yield ... **architecture**, with a **pipeline** configuration similar to that of ...

www.cs.virginia.edu/~techrep/CS-2005-11-rev.pdf - [Similar pages](#)

[PDF] **A SOFTWARE DEFINED COMMUNICATIONS BASEBAND DESIGN**

File Format: PDF/Adobe Acrobat - [View as HTML](#)